Accelerating Automotive Design with Arm POP IP

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Arm Taiwan Tech Symposia
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Automotive Design Requirements Overview

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Semiconductors in Automobiles

Advanced Driver Assistance Systems (ADAS)

- Sensing & imaging
- Safety & security
- Communication
- Navigation

Other In-Car Systems

- Comfort
- Infotainment
- Anti-lock braking
- Drive train efficiency

			2015		2020		2025
SAE* Level:	**0**	**1**	**2**	**3**	**4**	**5**
	No Automation	Drive Assistance	Partial Automation	Conditional Automation	High Automation	Full Automation

*Society of Automotive Engineers (SAE)

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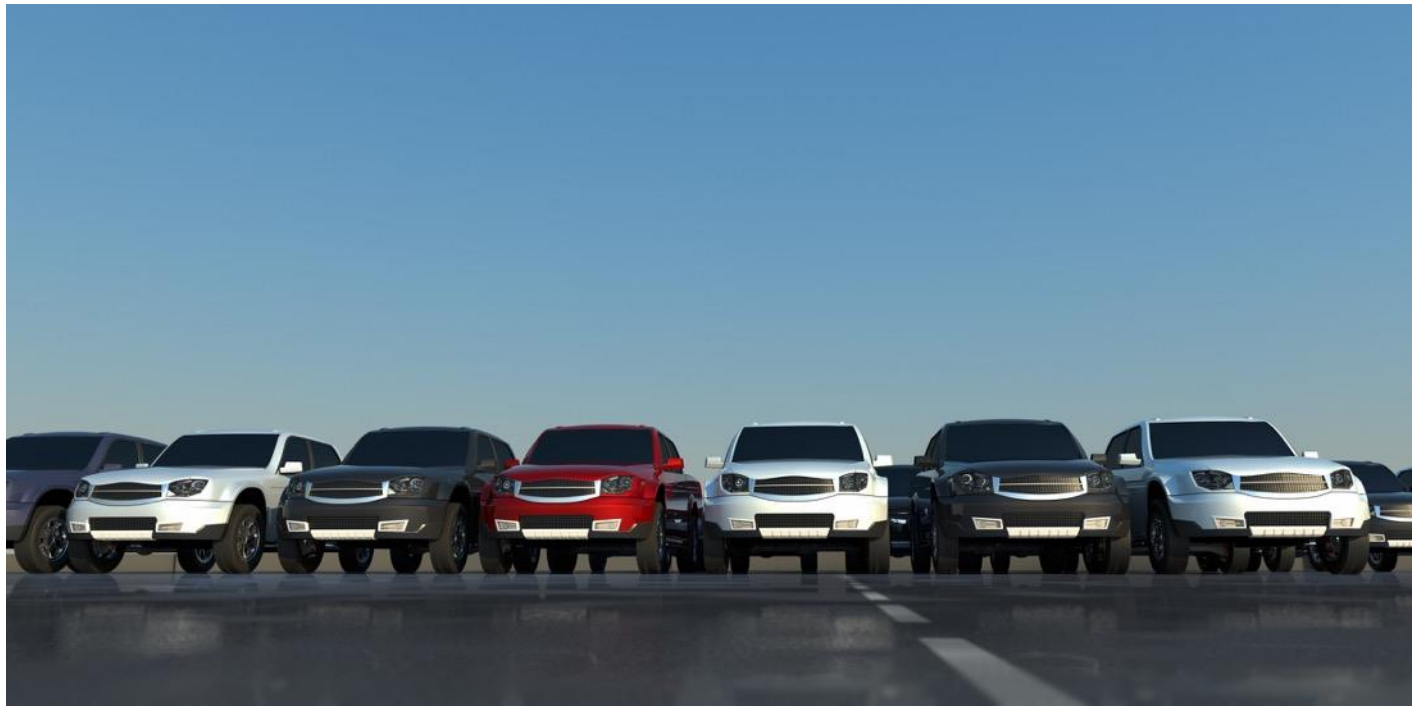
Main Considerations for Automotive SoC

- Developed to AEC-Q100 specifications
- ISO 26262 functional safety assessment and support for specific ASIL level
- Documented development process and quality control
- Optimize design for low PPM

Quality is the Challenge - Reliability is Key!

The quest for zero PPM



Example of an European car maker:

- 1.8M cars per year produced
- >1,000 semiconductors per car
- >1,8B semiconductors per year
- 1PPM failure would be 1,800 defective cars per year!
- Need zero defect!

Automotive: Safety and Reliability Requirements

Two Primary Standards for IP and SoC

ISO 26262

- Road vehicle electronics – Functional safety
- Safety Life Cycle
  - Concept phase through productization
- Automotive Safety Integrity Level (ASIL)-oriented and safety-oriented analysis
  - Safety levels ASIL A/B/C/D

AEC-Q100

- Failure Mechanism Based Stress Test Qualification for Integrated Circuits
- Defines grade levels
- Includes zero defects guidelines
- Qualification and requalification
  - Tests for ESD, LU, reliability, etc.

Physical IP Solutions

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Functional Validation

	Standard Cells	Memories
Extended Temperature Range	Functional validation at ≥150°C for automotive domain voltages.	Functional validation at ≥150°C for automotive domain voltages.
High Sigma Design Assurance	New High-Sigma Monte-Carlo validation capability for flop-flop and level-shifter functional validation.	5.4 sigma validation of read/write margin.
Transistor Aging	Toggle check at one PVT with uniformly aged transistor models.	Functional validation across PVT range with aged bit-cell models.

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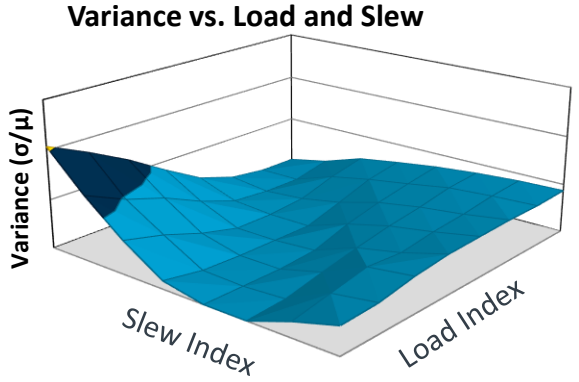
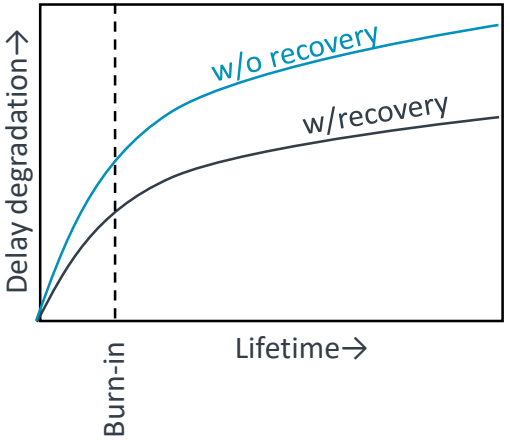
Static Timing

	Automotive Features
Extended Temperature Range	Extra PVT corners to validate timing at ≥150°C for automotive domain voltages.
On-Chip Variation	New support for Liberty Variance Format (LVF) libraries to accurately model process variation. Recommendations to margin for voltage & temperature variation are provided.
Transistor Aging	There no EDA support for static timing with aging so partners use proprietary methods. Arm is advocating for an EDA solution.





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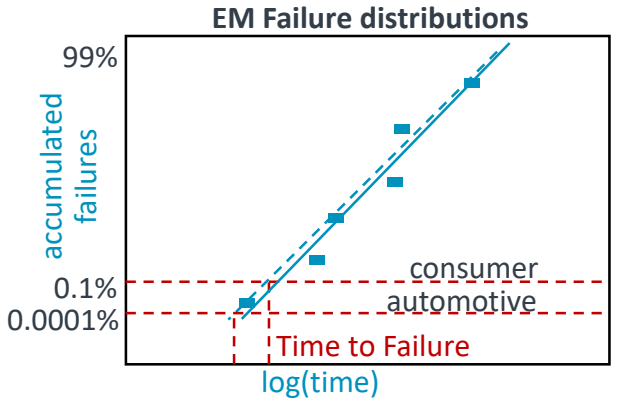
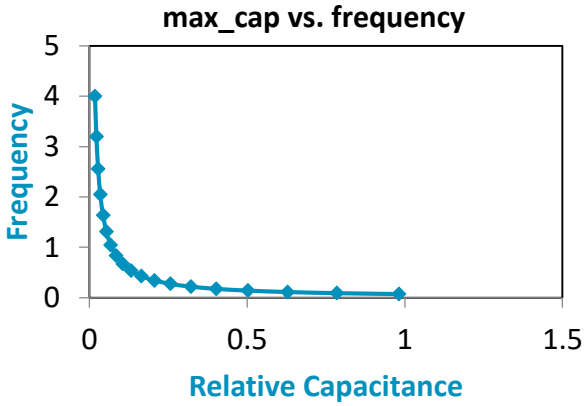
Reliability Assurance

	Automotive Features
1ppm Failure Rate	Foundries provide separate automotive EM tech files with 1ppm failure rate for physical IP validation.
Electromigration Model Generator (EMG)	EMG adds max cap tables in Liberty models to accurately constrain each cell. The tables can be scaled to support different mission profiles.
Memory EM	Designed to meet automotive EM current limits. Tables of maximum operating frequency indexed by time and temperature are available.
Oxide Breakdown	Library cells with extra line spacing can be provided to reduce the probability of Time Dependent Dielectric Breakdown (TDDB).





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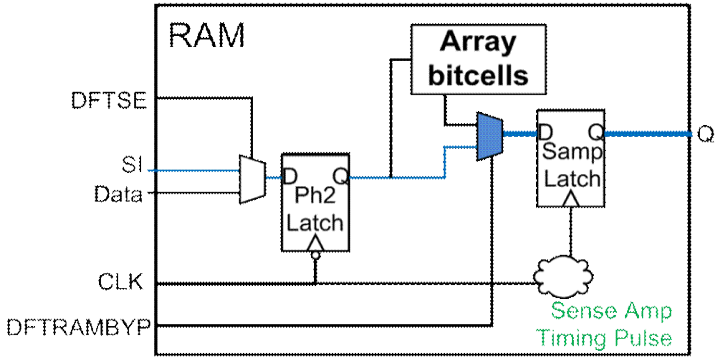
Post-Silicon Testability & Diagnosis

	Automotive Features
Full Scan in Memory	Added new memory compiler option to insert scan on all I/O pins providing full control and observation.
Cell-Aware ATPG	Added new view to boost fault coverage by creating patterns to expose faults on nets inside standard cells. Also enables fault location and diagnosis on silicon.
High Temperature Operating Life (HTOL)	Extra PVT corner to validate hold time at elevated temperature and voltage and ensure proper switching activity during qualification.
High Voltage Stress Test (HVST)	Optional PVT corner to validate hold time at elevated voltage during production testing.



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Functional Safety

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Functional Safety

- Systems that must function correctly to avoid unacceptable risk of damage or injury
  - Faults must be detected and controlled
  - Products must be properly specified and developed accordingly
- Safety critical
  - Braking, steering, acceleration, chassis control, air bag, seat belt
  - Driver relies on these systems to always function correctly
  - High safety integrity level (ASIL D)
- Safety ‘nominal’
  - Lane departure, speedometer, rear camera…
  - So long as the driver is made aware the system is not working
  - Medium safety integrity level (ASIL B)

Functional safety is the *absence of unreasonable risk* due to *hazards caused by malfunctioning behaviour of electrical / electronics systems*
ISO 26262 standard definition

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Functional Safety Requirements

- Quality criteria
- Errata management
- Training
- Documentation

- Version control
- Design criteria
- Design validation
- Deliverable validation

- Safety Manual
- Safety Verification
- ISO 26262 certification
- FEMA

Safety Manual	Includes automotive application information which is needed by SoC developers
Safety Verification	Includes safety goal verifications result which is needed by SoC developers
ISO 26262 **ASIL Assessment certification**	Covers reports by accredited independent 3rd-party assessor as minimum functional safety requirement
FMEA & FMEDA	Covers product release, defect reporting, root cause analysis, preventive actions

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Functional Safety Related Deliverables

Document or File Required	Work Requirement
Safety Package	See table below, standard deliverable to SoC designer
ISO 26262 ASIL assessment	Reports by accredited independent 3rd-party assessor.

Safety Package Content	Logic and GPIO libraries	MEM compilers
Safety Manual	Yes	Yes
Safety Case Summary Report	Yes	Yes
Safety Assessment Report	Yes	Yes
Verification Report	Yes (separate deliverables)	Yes (separate deliverables)
FMEDA / FMEDA report	Not applicable	Yes
FMEA / FMEA report	Only for audit	Only for audit
DFA / DFA report	Not applicable	Not applicable

Arm Automotive POP IP

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Transforming Auto with Optimized Physical IP & Design Focus

Automotive

Available

Optimized process **16FFC**

Optimized IP

- High temperature
- Fault tolerance
- Long lifetime
- Low power
- Certification

Early Development

Next Process

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Arm Artisan 16FFC Automotive Optimization

Leading US/Europe Automotive SoC company licensed Arm 16FFC Automotive platform

Close collaboration on features and procedures to ensure all safety and reliability requirements for automotive are fulfilled or exceeded

- AEC-Q100 Grade 1 compliant
- ISO 26262 certification and safety manuals
- Support of multiple voltage domains with 150ºC characterization

Optimized features for system ASIL-D qualification

- Development of dedicated “automotive only” memories with special features like full scan for all input pins for even higher reliability and testability

Design robustness for high temperature

- Memories margined for large temperature range
- Improved EM robustness on dedicated memories
- Logic cell for EM optimization with Electro-Migration Model Generator

Arm delivers “Safety Package” as part of the physical IP

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Automotive Performance Optimization Package (POP)

What's different?

Physical IP and Implementation Differences	Automotive POP	Standard POP
Temperature range	-40C to 150C	-40C to 125C
Voltage domains	Avoid over and underdrive	0.6V to 1.0V DVFS for peak performance
Logic Libraries	Focus on low power	9T – performance oriented
Signoff	LVF-based with signoff criteria designed to maximize reliability and yield	LVF based signoff criteria designed for high performance and yield
Memory / FCI	Highest testability	Standard memories
Frequency goal (typical)	Mid-range frequency at nom. domain	Above 2.5GHz at OD domain
EM optimization	Automotive requirements	10 years, 110C, OD
Other	Safety Package enabled	N/A

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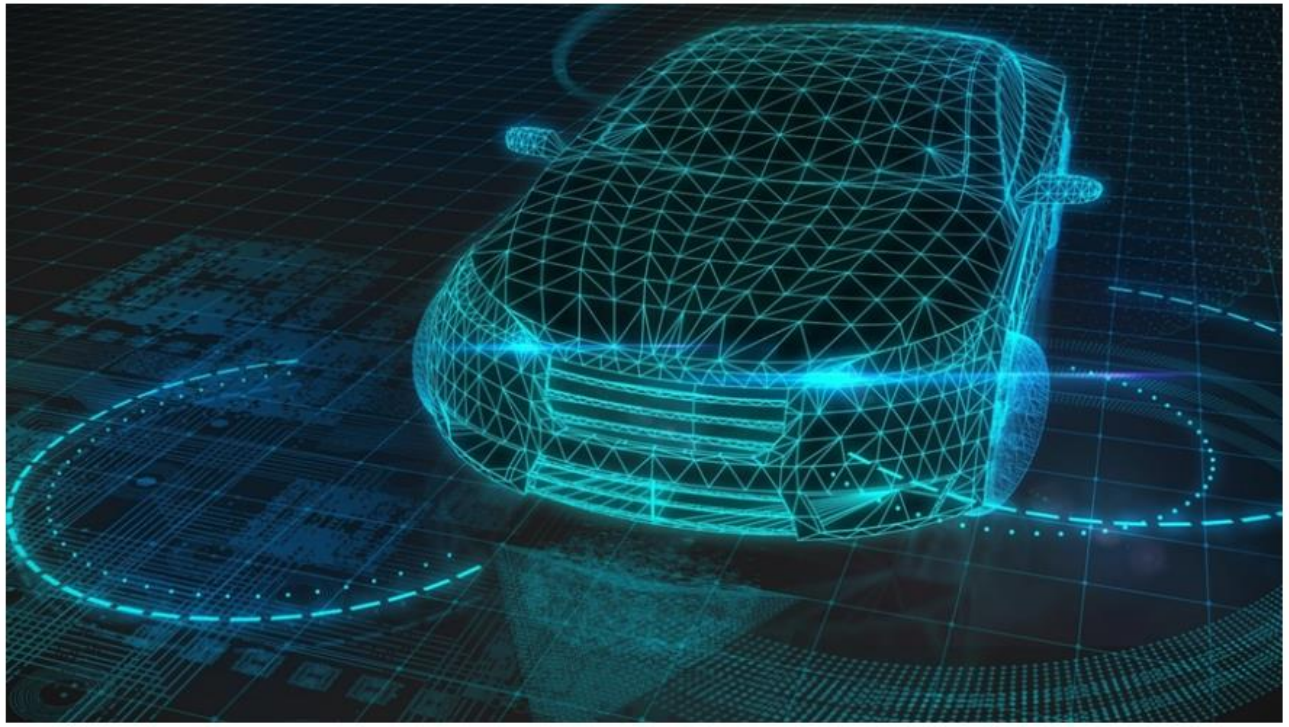
Arm enables NXP with dedicated automotive physical IP to address new feature and functionality demands



Safety is fundamental for advanced automotive applications and any IP considered for NXP's S32 Platform must not only take the future of automotive into consideration, but do so by meeting stringent automotive requirements to ensure we keep drivers, passengers and pedestrians safe,

Matt Johnson, senior vice president and general manager - Product Lines and Software, Auto MCU and Processors at NXP Semiconductors.

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Neubiberg, Mar. 22, 2018

Confirmation

To whom it may concern

exida.com GmbH hereby confirms that the Arm libraries and memory compilers for the TSMC CLN16FCLL001 process node, with versions:

- TSMC CLN16FCLL001 Standard Cell Libraries – see next page
- TSMC CLN16FCLL001 GPIO 1.8V TS74IG000 (r1p1)
- TSMC CLN16FCLL001 GPIO 3.3V TS74IG001 (r1p0)
- TSMC CLN16FCLL001 Ultra HD SP SRAM A1 MVt (r1p2)
- TSMC CLN16FCLL001 High Den SP SRAM A1 MVt (r1p1)
- TSMC CLN16FCLL001 Ultra HD 2 Port SRAM A1 MVt (r0p0)
- TSMC CLN16FCLL001 High Den SP RF A1 MVt (r1p1)
- TSMC CLN16FCLL001 High Speed 2 Port RF A1 MVt (r1p1)
- TSMC CLN16FCLL001 HD Limited Via ROM Auto1 MVt (r1p1)
- TSMC CLN16FCLL001 HD Via ROM Auto1 MVt (r0p1)
- TSMC CLN16FCLL001 UHD SP A1 SRAM SVt custom instance (r1p1)
- TSMC CLN16FCLL001 Ultra HD SP SRAM A1 SVt only (r0p1)

have been positively assessed according to the technical and functional safety management related requirements of ISO 26262 ASIL D in terms of the random integrity and the systematic capability.
The assessment took place between October 2017 and March 2018.

The assessment report and certificate will be issued within the next 3 months.

Assessor
Dipl.-Ing. (FH) Peter Müller

Assessor
Dipl.-Ing. (Univ.) Alexander Griesing

Successful ISO 26262 certification of Artisan IP by external accessor!

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Automotive IP solutions – Optimization at all Levels

- Automotive requirements are different, optimization is key
- Reliability requirements are stringent
- Functional safety is more and more important
- CPU implementation have different targets resulting in different results

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Start Your Designs with Arm Today - Talk to Us!

- Contact us at PDG-Mktg-Mgmt@arm.com for more information

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Multiple **FREE library programs** available now